CLAIMS

I/We claim:

[c1] 1. A memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory, each section having a row enable line for each row of the memory and a column enable line for each column of the memory for enabling access to a subdivision of a word of memory, each section having a section enable line for enabling access to that section;

for each row of each section, row enabler logic that enables the row enable line for that row of that section only when the section enable line for that section is enabled; and

for each section, column enabler logic that enables a column enable line for that section only when the section enable line for that section is enabled.

[c2] 2. The memory bank of claim 1 wherein the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port.

[c3] 3. The memory bank of claim 1 wherein different rows of different sections can be simultaneously accessed to satisfy different memory access requests.

[c4] 4. The memory bank of claim 1 wherein row and column address enable signals are buffered to accommodate row and column latencies.

[c5] 5. The memory bank of claim 1 including configuration information storage for selectively enabling sections.

[c6] 6. The memory bank of claim 5 wherein the memory bank is part of a multiport memory device and the selective enabling of sections is on a port-by-port basis.

[c7] 7. A memory bank having words that are addressable by addresses and having multiple sections, the memory bank comprising:

a plurality of sections, each section representing a subdivision of a word of memory, each word of memory being accessible via an address, each section being selectively enabled so that only a portion of a word corresponding to enabled sections is accessible so that sections that are not enabled use less power than sections that are enabled.

[c8] 8. The memory bank of claim 7 wherein the address is divided into a row portion and a column portion and the memory bank includes a row decoder and a column decoder to selectively accesses a word of the memory bank.

[c9] 9. The memory bank of claim 8 wherein output of the row decoder and output of the column decoder only drive sections that are enabled.

[c10] 10. The memory bank of claim 9 wherein the outputs are buffered to accommodate row and column latencies.

[c11] 11. The memory bank of claim 7 wherein the memory bank is part of a multiport memory device and wherein the section enable lines are enabled based on the accessing port.

[c12] 12. The memory bank of claim 7 wherein different rows of different sections can be simultaneously accessed to satisfy different memory access requests.

[c13] 13. The memory bank of claim 7 including configuration information storage for selectively enabling sections.

[c14] 14. The memory bank of claim 13 wherein the memory bank is part of a multiport memory device and the selective enabling of sections is on a port-by-port basis.